1. Features

- Low-voltage and Standard-voltage Operation
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- User-selectable Internal Organization
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- Three-wire Serial Interface
- Sequential Read Operation
- 2 MHz Clock Rate (5V)
- Self-timed Write Cycle (10 ms Max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Automotive Devices Available
- 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP and 8-ball dBGA2 Packages

2. Description

The AT93C56A/66A provides 2048/4096 bits of serial electrically erasable programmable read-only memory (EEPROM) organized as 128/256 words of 16 bits each (when the ORG pin is connected to VCC) and 256/512 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C56A/66A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead Ultra Thin mini-MAP (MLP 2x3), 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, and 8-ball dBGA2 packages.

The AT93C56A/66A is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable State. When CS is brought “high” following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C56A/66A is available in 2.7V to 5.5V and 1.8V to 5.5V versions.

Three-wire Serial EEPROM

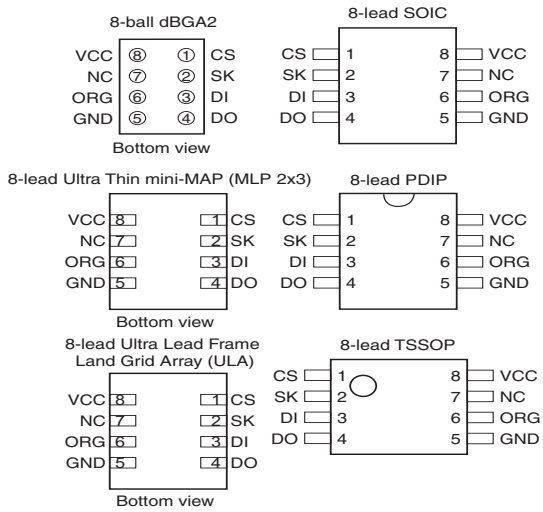
2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

AT93C56A
AT93C66A

Table 2-1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
NC	No Connect



3. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 3-1. Pin Capacitance(Note:)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 3-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V		0.4	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
V_{IL1}(Note:) V_{IH1}(Note:)	Input Low Voltage Input High Voltage	2.7V ≤ V_{CC} ≤ 5.5V		–0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}(Note:) V_{IH2}(Note:)	Input Low Voltage Input High Voltage	1.8V ≤ V_{CC} ≤ 2.7V		–0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA			0.4	V
			I_{OH} = –0.4 mA	2.4			V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA			0.2	V
			I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 3-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0		2 1 0.25	MHz
t_{SKH}	SK High Time	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 1000			ns
t_{SKL}	SK Low Time	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 1000			ns
t_{CS}	Minimum CS Low Time	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 400			ns
t_{PD1}	Output Delay to “1”	AC Test	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 1000	ns
t_{PD0}	Output Delay to “0”	AC Test	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 1000	ns
t_{SV}	CS to Status Valid	AC Test	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test $CS = V_{IL}$	$2.7V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			150 400	ns
t_{WP}	Write Cycle Time		$1.8V \le V_{CC} \le 5.5V$	0.1	3	10	ms
Endurance(Note:)	5.0V, 25°C			1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

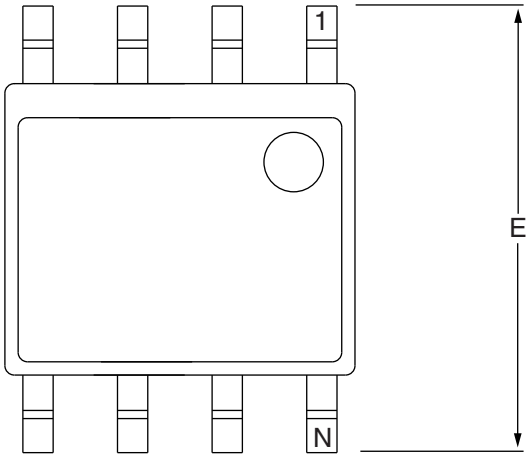
6. AT93C56A Ordering Information[1]

Ordering Code	Package	Operation Range
AT93C56A-10PU-2.7[2]	8P3	Lead-free/Halogen-free/ Industrial Temperature (−40°C to 85°C)
AT93C56A-10PU-1.8[2]	8P3	
AT93C56A-10SU-2.7[2]	8S1	
AT93C56A-10SU-1.8[2]	8S1	
AT93C56AW-10SU-2.7[2]	8S2	
AT93C56AW-10SU-1.8[2]	8S2	
AT93C56A-10TU-2.7[2]	8A2	
AT93C56A-10TU-1.8[2]	8A2	
AT93C56AU3-10UU-1.8[2]	8U3-1	
AT93C56AD3-10DH-1.8[3]	8D3	
AT93C56AY1-10YU-1.8[2] (Not recommended for new design)	8Y1	
AT93C56AY6-10YH-1.8[3]	8Y6	
AT93C56A-W1.8-11[4]	Die Sales	Industrial Temperature (−40°C to 85°C)

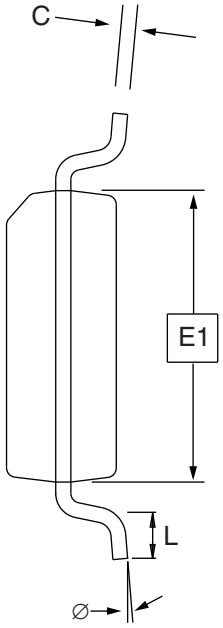
Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC characteristics table.
2. “U” designates Green package + RoHS compliant.
3. “H” designates Green package + RoHS compliant, with NiPdAu Lead Finish.
4. Available in waffle pack and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8U3-1	8-ball, die Ball Grid Array Package (dBGA2)
8Y1	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead package (DFN), (MLP 2x3 mm)
8D3	8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)
Options	
–2.7	Low-voltage (2.7V to 5.5V)
–1.8	Low-voltage (1.8V to 5.5V)

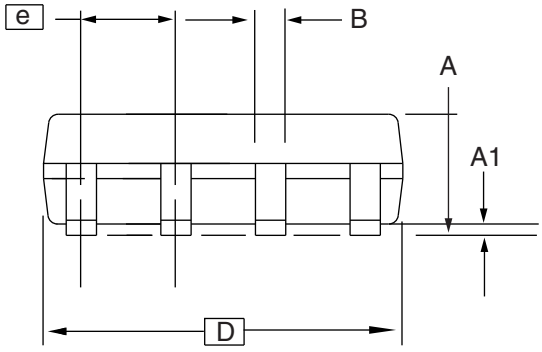
8.2 8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

8.3 8S2 – EIAJ SOIC